



Efficient Implementation of Filtering and Resampling Operations on Field Programmable Gate Arrays (FPGAs) for Software Defined Radio (SDR).

Georgios Giannoulis

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In Software Defined Radios a good portion (or even the entirety) of the modulation and demodulation processes is performed in the digital domain. The data rate of the transmitted information is very important, since efficiency is a key requirement in real time implementations and cost increases considerably with the number of samples per second to be processed. In this thesis, we address the problem of efficient design of the resampling operations, so that they can be implemented on Field Programmable Gate Arrays (FPGAs). A set of filtering and resampling operations is developed in the Simulink environment through Xilinx/Simulink blocksets, where all the included subsystems of the design are fully accessible by the designer in any stage of operation. The key ingredient is the use of a Multiplier and Accumulator (MAC) architecture, which can be either time multiplexed for maximum hardware efficiency, or run on a parallel structure for maximum time efficiency.

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